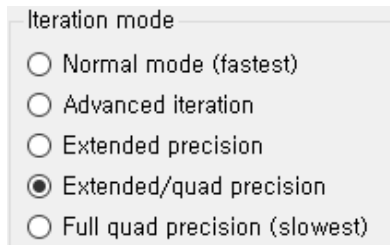


Simulation Environment Before Simulator

1. Open windows explorer or click on My Computer or open other file manager of your choice.
2. Should be pick the file ([pspice_dig.lib](#) in attached) up and drop into the My Computer > Windows > Program files > SIMetrix900 > support > models folder before the simulation run

To replace the PSpice digital model file (pspice_dig.lib) with SIMetrix subcircuit equivalents for onsemi isolated gate driver models.

3. Recommended use the simulator conversion option below.



NCP51152 Simetrix model

1. The schematic and simulation is ready to use with SIMetrix 9.0.
2. The user should be able to simulate by pressing the run button.
3. If the NCP51152 is accidentally deleted the user must take the following steps or down load the schematic again
 1. Install the Library
 1. File > Model Library > add/ remove Libraries.
 2. Point the location that the NCP51152 Simulation files were saved during download.
 3. Ensure models are added to the current selected libraries by using the arrows on the select libraries tab.
4. Included models
 1. NCP51152AA for 6.0-V V_{CC} UVLO with respect to VEE and split outputs (OUTH & OUTL).
 2. NCP51152AB for 6.0-V V_{CC} UVLO with respect to GND2 pin and negative bias pin (VEE).
 3. NCP51152BA for 8.7-V V_{CC} UVLO with respect to VEE and split outputs (OUTH & OUTL).
 4. NCP51152BB for 8.7-V V_{CC} UVLO with respect to GND2 pin and negative bias pin (VEE).
 5. NCP51152CA for 12-V V_{CC} UVLO with respect to VEE and split outputs (OUTH & OUTL).
 6. NCP51152CB for 12-V V_{CC} UVLO with respect to GND2 pin and negative bias pin (VEE).
 7. NCP51152DA for 17-V V_{CC} UVLO with respect to VEE and split outputs (OUTH & OUTL).
 8. NCP51152DB for 17-V V_{CC} UVLO with respect to GND2 pin and negative bias pin (VEE).
 9. ONSEMI_SiCMOSFET_1200M3S

Exclusions from the model

- Thermal behavior is not modeled.